REMARKS

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received.

The applicants acknowledge and appreciate receiving an initialed copy of the form PTO-1449 that was filed on 21 October 2003

Claims 1-12 are pending. Claims 10-12 are new. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 1-9 were rejected under 35 USC 102(b) as being anticipated by the patent to Nakano. The applicants respectfully request that this rejection be withdrawn for the following reasons.

In the device of claim 1, an output voltage forming circuit, a ground wiring pattern, and a common ground wiring pattern are formed in layers of a multi-layered substrate. The ground wiring pattern is connected with the common ground wiring pattern via a connecting part. The patent to Nakano fails to disclose such an arrangement. That is, the patent to Nakano does not disclose that the buffer amplifier 11 and the ground wire 21 are formed in layers of a multi-layer

substrate. For these reasons, the applicants respectfully request that the rejection of claims 1-9 be withdrawn.

Further, with regard to claims 5 and 6, although discloses an arrangement of the ground wire 21 and a ground wire 14 connected with a bonding wire 22, Nakano fails to disclose interlayer connection between the ground wires 14, 21.

Claims 10-12 are new. Claims 10-12 depend on claim 1 and are considered to be patentable for the reasons given above with respect to claim 1.

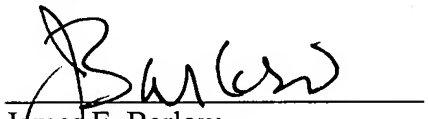
With regard to claims 10 and 11, the output voltage forming circuit and the ground wiring pattern are formed in the same layer or the ground wiring pattern is in the layer immediately below the layer of the output voltage forming circuit. That is, the output voltage forming circuit and the ground wiring pattern are closely arranged so that the influence of potential variation that occurs in the ground wire with respect to the common wiring pattern is reduced.

In addition, with regard to claim 12, the ground wiring pattern of the present invention has a smaller impedance that the connecting part. Thus, a potential variation that occurs in the ground wiring pattern is less likely to affect the common ground wiring pattern. A bonding wire such as the bonding wire 22 disclosed by Nakano generally has a small impedance. Thus, a potential variation that occurs in the ground wire 21 of the buffer amplifier 11 is more likely to affect the ground wire 14.

In view of the foregoing, the applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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